REMARKS

In the Official Action mailed on **April 7, 2004,** the Examiner reviewed claims 1, 3-14, and 16-21. Claims 1, 3-14, and 16-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nakajima (USPN 5,269,012, hereinafter "Nakajima") in view of Chen et al. (USPub 2003/0120879 A1, hereinafter "Chen").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 9, and 14 were rejected as being unpatentable over Nakajima in view of Chen. Examiner avers "Chen's linked list system does not make a reference to a system clock for operation (asynchronously)." Applicant respectfully points out that the system of Chen does not teach communications **between cells** within the linked list—either synchronous or asynchronous. In the system of Chen, the communications are between the processor and the queue memory. The communications between the processor and the queue memory are addressed in chunks under control of the processor (see Chen paragraph [0032]). It is well known in the art that when a processor addresses memory, one or more clock signals are involved. These clock signals typically include a row-address strobe (RAS) and a column-address strobe (CAS).

In contrast, the present invention **moves signals between cells** within the last-in, first-out buffer without reference to any external clock signals (see FIGs. 11A-D, and page 21, line 16 to page 22, line 16 of the present invention). Once data has been placed within an input cell, the data moves to and between cells in the substack without reference to any external clock signals such as RAS and CAS.

Moving data between cells without reference to an external clock is an advantage because it allows data motion between elements of the stack without waiting for a next clock signal and address strobe. Note that in an asynchronous

system, data items can ripple through stack cells without having to wait for worst case propagation delays as in a synchronous system. Moreover, it is not obvious to create the rather complicated asynchronous control structures for an asynchronous stack that are illustrated in FIGs. 1-19 of the instant application.

There is nothing within Nakajima or Chen, either separately or in concert, which suggests operating asynchronously. In fact, both Nakajima and Chen disclose a synchronous circuit driven by a clock, which teaches away from the instant invention.

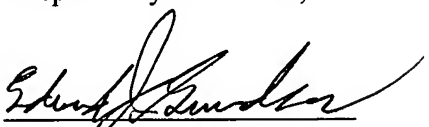
Accordingly, Applicant has amended independent claims 1, 9, and 14 to clarify that the present invention moves signals **between cells** within the last-in, first-out buffer without reference to any external clock signals.

Hence, Applicant respectfully submits that independent claims 1, 9, and 14 as presently amended are in condition for allowance. Applicant also submits that claims 3-8, which depend upon claim 1, claims 10-13, which depend upon claim 9, and claims 16-21, which depend upon claim 14, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 
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